IFW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Turner, Steven E.	Appl No.:	10/593,807
Filed:	9/21/06	Dkt. No:	20040084 US
For:	Single-Level Parallel-Gated Carry/Majority Circuits And Systems Therefrom		

CERTIFICATE OF MAILING 37 CFR 1.8: I certify that this correspondence is being deposited on the below date with the U.S. Postal Service with sufficient postage as FIRST CLASS MAIL addressed to: Mail Stop Amendment, Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450.

Date: 3/27/07 Maureen Miles

Maureen Miles

Dear Commissioner:

INFORMATION DISCLOSURE STATEMENT

Applicants submit this statement in accordance to the duty of disclosure under 37 C.F.R. §§1.56, 1.97, and 1.98, and requests consideration of this Information Disclosure Statement.

Compliance with 37 C.F.R. §1.97: This Information Disclosure Statement is filed within three (3) months of the filing date of a National Application or before the mailing date of a first office action on the merits. No fee or certification is required.

Information Cited: The Applicants hereby make of record in the above-identified application, the information listed on the attached forms PTO-08A and PTO-08B. The order of presentation of the references should not be construed as an indication of the importance of the reference. As all the references listed on attached forms PTO-08A and PTO-08B are in English, no commentary is required.

Remarks: Pursuant to 37 CFR 1.98 (a)(2)(i) applicant has not transmitted herewith copies of cited U.S. Patents and U.S. patent application publications as the above application was filed after June 30, 2003. Applicants respectfully request that:

1. The Examiner consider completely the cited information, along with any other information, in reaching a determination concerning the patentability of the present claims;

2. The enclosed forms PTO-08A and PTO-08B be signed by the Examiner to evidence that the cited information has been fully considered by the Patent and Trademark Office during the examination of this application; and

3. The citations for the information be printed on any patent which issues from this application.

By submitting this Information Disclosure Statement, the Applicants make no representation that a search has been performed, of the extent of any search performed, or that more relevant information does not exist.

By submitting this Information Disclosure Statement, the Applicants make no representation that the information cited in the Statement is, or is considered to be, material to patentability as defined in 37 C.F.R. §1.56(b).

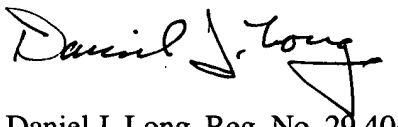
By submitting this Information Disclosure Statement, the Applicants make no representation that the information cited in the Statement is, or is considered to be, in fact, prior art as defined in 37 C.F.R. §102.

Notwithstanding any statement by the Applicant, the Examiner is urged to form his own conclusion regarding the relevance of the cited information.

An early and favorable action is hereby requested.

Please enter in the above application and communicate in all related matters with the undersigned. All necessary fees are intended to be included, however the Office is hereby authorized to charge any deficiency or credit any overpayment in the fees to deposit account #190130.

Respectfully submitted,



Daniel J. Long, Reg. No. 29,404

BAE SYSTEMS
65 Spit Brook, Road, NHQ01-719
Nashua, NH 03061
Tel. No. (603) 885-2643
Fax. No. (603) 885-2167
Email: Daniel.j.long@baesystems.com

Form PTO-08A				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	10/593,807
				Filing Date	9/21/06
				First Named Inventor	Turner, Steven E.
				Group Art Unit	
				Examiner Name	
Sheet	1	of	1	Attorney Docket Number	20040084 US

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	U.S. Patent Document Number	Code	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		5,577,199		Tanabe, et al.	11-19-1996	
		6,008,670		Pace, et al.	12-28-1999	
		6,262,604 B1		Gabet, et al.	07-17-2001	
		6,347,325 B1		Ribner, et al.	02-12-2002	
		6,366,174 B1		Berry, et al.	04-02-2002	
		6,704,761 B1		Farrokh, et al.	03-09-2004	
		3,248,529		Buelow, et al.	04-26-1966	
		US2002/0198912 A1		Humphreys, et al.	12-26-2002	

FOREIGN PATENT DOCUMENTS

Examiner Initials	Cite No.	Foreign Patent Document Office Code	Number	Kind	Name of Patentee or Applicant of Cited Document		Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T

Examiner Signature		Date Considered	

* EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.

Form PTO-08B				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	10/593,807
				Filing Date	9/21/06
				First Named Inventor	Turner, Steven E.
				Group Art Unit	
				Examiner Name	
Sheet	1	of	1	Attorney Docket Number	20040084 US

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	(Including Name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc...), date, page(s), volume-issue number(s), publisher, city, and/or country where published.	T
		TURNER, ET AL., Benchmark Results For High-Speed 4-Bit Accumulators Implemented In Indium Phosphide DHBT Technology, IEEE Lester Eastman Conference on High Performance Devices, Rensselaer Polytechnic Institute, August 4-6, 2004	
		GUTIERREZ-AITKEN, ET AL., Ultrahigh-Speed Direct Digital Synthesizer Using InP DHBT Technology, IEEE Journal of Solid-State Circuits, Vol. 37, No. 9, September 2002, pp 1115-1119	
		HE, ET AL., Self-Aligned InP DHBT With f_t and f_{max} Over 300 GHz in a New Manufacturable Technology, IEEE Electron Device Letters, Vol. 25, No. 8, August 2004, pp 520-522	
		EKROOT, ET AL., A GaAs 4-bit Adder-Accumulator Circuit for Direct Digital Synthesis, IEEE Journal of Solid-State Circuits, Vol. 23, No. 2, April 1988, pp 573-580	
		TURNER, ET AL., 4-Bit Adder-Accumulator at 41-GHz Clock Frequency in InP DHBT Technology, IEEE Microwave and Wireless Components Letters, 2005, pp 1-3	
		MATHEW, ET AL., 2-Bit Adder Carry and Sum Logic Circuits Clocking at 19 GHz Clock Frequency in Transferred Substrate HBT Technology, Dept of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106, GTRAN Inc, Newbury Park, CA 91320	
		DVORAK, ET AL., 300 GHz InP/GaAsSb/InP Double HBTs with High Current Capability and $BV_{CEO} \geq$ 6V, IEEE Electron Device Letters, Vol. 22, No. 8, August 2001, pp 361-363	
		SALOUS, ET AL., FPGA-based Hybrid Accumulator Architecture for Digital Chirp Synthesis, Int. J. Electronics, 1996, Vol. 80, No. 3, pp 441-447	
		BETOWSKI, ET AL., Considerations for Phase Accumulator Design for Direct Digital Frequency Synthesizers, School of Electrical Engineering & Computer Science, Washington State University, Pullman, WA 99164	
		MATHEW, ET AL., 2-Bit adder: Carry and Sum Logic Circuits at 19 GHz clock frequency in InAlAs/InGaAs HBT Technology, Electronics Letters, Vol. 37, No. 19, September 13, 2001, pp 1156-1157	

Examiner Signature		Date Considered	

* EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.